AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A compound semiconductor FET comprising:

an undoped AlN layer provided on a substrate;

a plurality of III-N layers provided on the AlN layer, the III-N layers including an undoped GaN layer;

an n-type delta doped ~~III-N~~ GaN layer interposed between the undoped AlN layer and the ~~plurality of III-N layers~~ undoped GaN layer, and having dopant concentration for reducing discontinuity of an electric field at an interface between the AlN layer and the ~~III-N layers~~ the undoped GaN layer;

a source electrode;

a gate electrode; and

a drain electrode.

2. (Original) The compound semiconductor FET according to claim 1, wherein the n-type delta doped III-N layer is an n-type delta doped GaN layer,

wherein the plurality of III-N layers comprise a GaN layer and an AlGaN layer formed on the GaN layer, and

wherein the source electrode, the gate electrode, and the drain electrode are provided on the AlGaN layer.

3. (Previously Presented) The compound semiconductor FET according to claim 1, further comprising an insulating layer on an uppermost layer of the plurality of III-N layers, wherein the n-type delta doped III-N layer is an n-type delta doped GaN layer,

wherein the plurality of III-N layers comprise a GaN layer and an AlGaN layer formed on the GaN layer,

wherein the source electrode and the drain electrode are provided on the AlGaN layer, and

wherein the gate electrode is provided on the insulating layer.

4. (Canceled)

5. (Previously Presented) The compound semiconductor FET according to Claim 1, wherein material of the substrate is sapphire,

wherein each of the semiconductor layers formed upon the substrate is of a C-plane Ga-surface type, and

wherein sheet doping concentration of the n-type delta doped III-N layer is within a range of 1×10^{13} cm^{-2} to 2×10^{13} cm^{-2}.

6. (Previously Presented) The compound semiconductor FET according to Claim 1, wherein material of the substrate is SiC,

wherein each of the semiconductor layers formed upon the substrate is of a C-plane Ga-surface type, and

wherein sheet doping concentration of the n-type delta doped III-N layer is within a range of 5×10^{12} cm^{-2} to 1.5×10^{13} cm^{-2}.

7. (Original) An electronic circuit provided with the compound semiconductor FET as defined in claim 1.